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15EC61

Sixth Semester B.E. Degree Examination, June/July 2019
Digital Communication

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Determine the Hilbert transform of the signal g(t) = sin c(t). **(04 Marks)**

b. Determine the pre-envelope and complex envelope of the signal shown in Fig.Q1(b). **(06 Marks)**

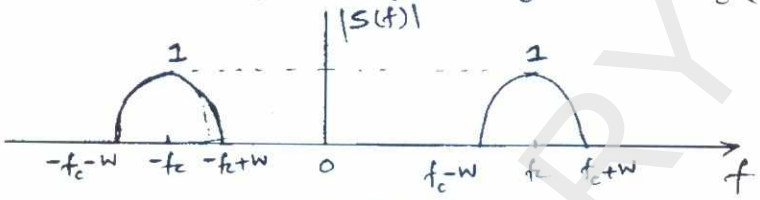

Fig.Q1(b)

c. Explain the time–domain procedure for the complex representation of band pass signals and systems. **(06 Marks)**

OR

2 a. For a binary sequence 0100000001011 construct i) RZBipolar format ii) Manchester format iii) B3Zs format iv) B6ZS format v) HDB3 format.
Also mention the application of B3ZS and B6ZS formats. **(07 Marks)**

b. Draw the power spectra of : i) RZAMI signal ii) NRZ polar signal. **(03 Marks)**

c. Consider a bandpass signal S(t) which is represented in terms of in-phase and quadrature components. Suggest a suitable scheme for :
i) extracting the in-phase and quadrature components from the band pass signal
ii) reconstructing the band pass signal from in-phase and quadrature components. **(06 Marks)**

Module-2

3 a. For the signals $s_1(t)$, $s_2(t)$, $s_3(t)$ and $s_4(t)$ shown in Fig.3(a), find a set of orthonormal basis functions using gram–Schmidt orthogonalization procedure. **(09 Marks)**

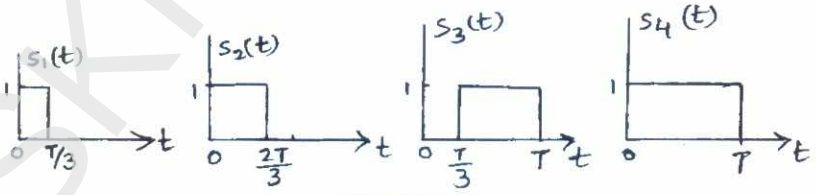

Fig.Q3(a)

b. Explain with neat diagram and necessary equations the matched filter receiver. **(07 Marks)**

OR

4 a. Obtain the decision rule for maximum likelihood decoding and explain the correlation receiver. **(08 Marks)**

b. Show that for a noisy input, the mean value of the j^{th} correlator output X_j depends only on S_{ij} and all the correlators outputs X_j, j = 1, 2, - - - - , N, have a variance equal to the PSD No/2 ofthe additive noise process w(t). **(08 Marks)**

Module-3

5 a. Sketch the QPSK wave form for the sequence 01101000. **(06 Marks)**

b. Obtain the expression for average probability of symbol error for BPSK using coherent detection. **(06 Marks)**

c. Obtain the constcleation of QAM for M = 16 and draw the signal space diagram. **(04 Marks)**

OR

6 a. Explain the generation and coherent detection of BFSK system. **(06 Marks)**

b. The binary sequence 1100100010 is applied to the DPSK transmitter

i) Sketch the resulting wave from at the transmitter output.

ii) Applying this waveform to the DPSK receiver, show that in the absence of noise, the original binary sequence is reconstructed at the receiver output. **(06 Marks)**

c. An FSK system transmits binary data at the rate of 2×10^6 bps. During the source of transmission, AWGN of zero mean and two sided PSD 10^{-20} Watts/Hz is added to the signal. The amplitude of the received sinusoidal wave for digit 1 or 0 is 1μv. Determine the average probability of symbol error assuming non-coherent detection. **(04 Marks)**

Module-4

7 a. Explain the following terms with related equations and diagram with respect to base band transmission.

i) ISI and Nyquist condition for zero ISI

ii) Duobinary signal pulse

iii) Modified duobinary signal pulse

iv) Partial response signals

v) Raised cosine spectrum. **(10 Marks)**

b. Explain the need for precoder in a duobinary signaling. The binary sequence 111010010001101 is the input to the precoder whose output is used to modulate a duobinary transmitting filter. Obtain the precoded sequence, transmitted amplitude levels, the received signal levels and the decoded sequence. **(06 Marks)**

OR

8 a. With a neat diagram, explain the concept of linear traversal filter. **(06 Marks)**

b. Consider a channel distorted pulse x(t), at the input to the equalizer, given by $x(t) = \frac{1}{1+\left(\frac{2t}{T}\right)^2}$ where 1/T is the symbol rate. The pulse is sampled at the rate 2/T and equalized by a zero-forcing equalizer. Determine the coefficients of a five-tap zero-forcing equalizer. **(06 Marks)**

c. Write a note on eye diagram. **(04 Marks)**

Module-5

9 a. With a neat diagram explain the generation of PN sequences and state its properties. **(06 Marks)**

b. A DS spread–spectrum signal is designed so that the power ratio P_R/P_N at the intended receiver is 10^{-2}. If the desired $E_b/N_0 = 10$ for acceptable performance, determine the minimum value of the processing gain. **(04 Marks)**

c. Explain with neat block diagram FH spread –spectrum system. **(06 Marks**

OR

10 a. Explain the generation and demodulation of DS spread spectrum signal. **(06 Marks)**

b. Write a note on application of spread spectrum in wireless LANs. **(04 Marks)**

c. With a neat block diagram, explain the IS–95 reverse link. **(06 Marks)**

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15EC62

Sixth Semester B.E. Degree Examination, June/July 2019
ARM Micro Controller and Embedded Systems

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain the architecture of ARM cortex – M3 processor with neat diagram. **(08 Marks)**
b. With neat diagram, explain operation mode and privilege levels in cortex M3. **(08 Marks)**

OR

2 a. What is stack? Explain push and pop operation. With the help of a neat diagram. **(07 Marks)**
b. Explain in detail special registers used in ARM cortex M3 processor. **(09 Marks)**

Module-2

3 a. Write an ALP to calculate the sum of 1 to 10 numbers. **(08 Marks)**
b. Explain the following instruction set : i) BFC ii) SBFX iii)ASR iv) MRS. **(04 Marks)**
c. Explain how CMSIS provides standard access. Interface for Embedded software. **(04 Marks)**

OR

4 a. Write a program to blink a LED using 'C' language. **(08 Marks)**
b. Explain the following assembler directives AREA, ENTRY, DCB, ALIGN. **(04 Marks)**
c. Explain different bus interfaces supported by cortex M3. **(04 Marks)**

Module-3

5 a. Explain how embedded system are classified. **(08 marks)**
b. With neat block diagram, explain the element of embedded system. **(08 Marks)**

OR

6 a. Differentiate between RISC and CISC. **(04 Marks)**
b. Explain how program memory are classified. **(08 Marks)**
c. Explain how brown-out protection circuits works. **(04 Marks)**

Module-4

7 a. What are the operational and nonoperational attributes of an embedded systems. **(10 Marks)**
b. Explain different types of serial interface bus used in automotive communication. **(06 Marks)**

OR

8 a. Explain fundamental issues in hardware software co-design. **(06 Marks)**
b. Explain with a neat block diagram how source file to object file translation take place. **(06 marks)**
c. Explain super loop based approach of embedded firmware design. **(04 Marks)**

Module-5

9 a. With neat diagram explain operating system architecture. **(08 marks)**

b. Explain how operating systems are classified. **(04 marks)**

c. Differentiate between hard real time system and soft real time system with an example for each. **(04 Marks)**

OR

10 a. With neat diagram, explain embedded system development environment. **(08 marks)**

b. For the following jobs calculate the turnaround time, waiting time using preemptive SJF scheduling algorithm. **(04 Marks)**

Jobs	CPU bust time	Arrival time
1	10	0.0
2	2	3.0
3	1	4.0
4	4	5.0

c. Write a note on IAP [In Application Programming] and in system programming. **(04 Marks)**

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15EC63

Sixth Semester B.E. Degree Examination, June/July 2019
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Derive the CMOS inverter DC characteristics graphically from p device and n device characteristics and show all operating regions. **(08 Marks)**

b. Explain the working of nMOS enhancement mode transistor with suitable diagrams. **(08 Marks)**

OR

2 a. Derive expression for drain current in linear and saturation region for nMOS transistor. **(08 Marks)**

b. With neat sketches explain the CMOs P-well process steps to fabricate a CMOS inverter. **(08 Marks)**

Module-2

3 a. Write the lambda based design rules for separation of layers and transistors. **(06 Marks)**

b. Draw circuit, stick and layout diagram for nMOS shift register cell. **(10 Marks)**

OR

4 a. Define sheet resistance (R_S) standard unit of capacitance ($\square C_g$) and delay unit (τ) **(06 Marks)**

b. Calculate the capacitance of the structure given below in Fig.Q4(b). **(10 Marks)**

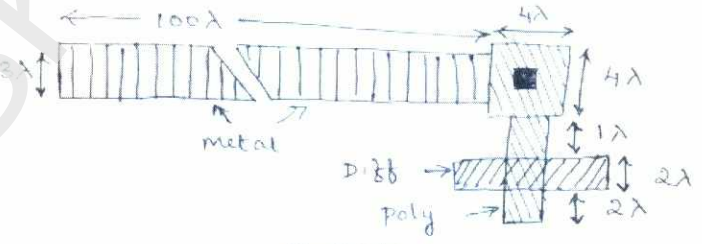

Fig.Q4(b)

Area capacitance value for metal 1 to substrate = 0.3pF × 10^{-4}/μm^2(0.075 relative value)
Area capacitance value for diffusion to substrate = 1pf × 10^{-4}/μm^2(0.25 relative value)
Area capacitance value for polysilicon to substrate = 0.4 pF × 10^{-4}/μm^2(0.1 relative value).

Module-3

5 a. Obtain the scaling factor for the following device parameters :
   i) gate capacitance
   ii) gate area
   iii) saturation current (Idss)
   iv) channel resistance (R_{on})
   v) maximum operating frequency (f_0)
   vi) power dissipation per gate (P_g)
   vii) current density (J)
   viii) gate delay (T_d). **(08 Marks)**

   b. With a neat diagram explain 4 × 4 Barrel shifter. **(08 Marks)**

OR

6 a. Explain the general arrangement of a 4 bit data path for processor. **(08 marks)**

   b. Describe Manchester carry chain element. **(08 Marks)**

Module-4

7 a. Discuss the architectural issues to be followed in the design of VLSI sub system. **(05 Marks)**

   b. Explain in detail the general structure of an FPGA fabric. **(06 Marks)**

   c. Explain switch logic implementation of CMOS 5 way selector with neat circuit diagram. **(05 Marks)**

OR

8 a. Explain the structured design approach for the implementation of a parity generator. **(08 marks)**

   b. Explain dynamic CMOS logic with example. **(08 Marks)**

Module-5

9 a. Explain 3 transistor dynamic RAM cell with schematic diagram. **(06 Marks)**

   b. Explain any two fault models in combinational circuits. **(06 Marks)**

   c. Write a note on automatic test pattern generation. **(04 Marks)**

OR

10 a. write short notes on :
   i) observability and controllability
   ii) Built In Self Test (BIST). **(08 Marks)**

   b. Explain nMOS pseudo static RAM cell with schematic diagram. **(08 Marks)**

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15EC64

Sixth Semester B.E. Degree Examination, June/July 2019
Computer Communication Networks

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Compare and contrast byte – stuffing and bit stuffing. **(06 Marks)**

b. With a neat diagram, explain encapsulation and decapsulation in protocol layering. **(04 Marks)**

c. With a layer diagram, explain the responsibilities of each layer in TCP/IP protocol suite. **(06 Marks)**

OR

2 a. Discuss the ARP operation and show how ARP sends request and reply message with an example. **(08 Marks)**

b. Explain stop and wait protocol and show how adding sequence numbers can prevent duplicates with the help of flow diagram. **(08 Marks)**

Module-2

3 a. Explain the behaviour of CSMA protocol with a neat diagram and show the vulnerable time in CSMA. **(08 Marks)**

b. A pure ALOHA network transmits 200-bit frames on a shared channel of 200kbps. What is through put if the system (all stations together) produces?

i) 1000 frames per second?

ii) 500 frame per second? **(04 Marks)**

c. Explain reservation as a controlled access method. **(04 Marks)**

OR

4 a. Explain the format of standard Ethernet frame. What are the minimum and maximum frame lengths? **(07 Marks)**

b. Identify if the following Ethernet MAC addresses are unicast, multicast or broadcast

i) 47 : 20 : 1B : 2E : 08 : EE

ii) EE : FF : 10 : 01 : 11 : 00

iii) FF : BF : FF : FF : FF : FF **(03 Marks)**

c. What are the two effects of the bridges on an Ethernet LAN? Explain with a neat diagram. **(06 Marks)**

Module-3

5 a. With a neat diagram, explain two types of networks defined in Bluetooth. **(04 Marks)**

b. What is hidden station problem in wireless LAN's? Give solution for it. **(06 Marks)**

c. Describe WLAN. How is it used in grouping of stations? **(06 Marks)**

OR

6 a. Explain the occupation of the address space in classful addressing. **(04 Marks)**

b. A block of addresses is granted to a small organization. We know that one of the addresses is 167·199·170·82/27. What is the first address, last address and total number of address of the block? **(06 Marks)**

c. With a neat diagram, explain how can a NAT help in address translation. **(06 Marks)**

Module-4

7 a. With a neat diagram explain IPV4 datagram format? **(08 Marks)**

b. What is the two addresses approach in mobile host? Explain the significance of home agent and foreign agent with a diagram. **(08 Marks)**

OR

8 a. With relevant diagrams describe Distance Vector Routing. What is two node instability in DVR? **(10 Marks)**

b. Explain operation of Border Gateway Protocol (BGP) with a diagram. **(06 Marks)**

Module-5

9 a. Explain connection less and connection oriented service showing the movement of packets using time line. **(08 Marks)**

b. Explain why the size of the send window in Go back N must be less than 2^m? **(08 Marks)**

OR

10 a. Explain TCP connection establishment and connection termination using three way hand shaking. **(10 Marks)**

b. Describe slow start algorithm for handling congestion in TCP. **(06 Marks)**

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15EC654

Sixth Semester B.E. Degree Examination, June/July 2019
Digital Switching Systems

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. With a neat diagram explain the working principle of four wire circuit. Also give the equations for echoes. **(10 Marks)**

b. Explain the hierarchy of national public switched telecommunication network with neat diagram. **(06 Marks)**

OR

2 a. Explain in brief, the regulation and standards in telecommunication network. **(08 Marks)**

b. Express the following power levels in dBm and dBw. i) 1mW ii)1W iii)2mW iv) 100mW. **(08 Marks)**

Module-2

3 a. Explain the functions of switching system. **(08 Marks)**

b. Explain the working of distribution frame in strowger exchange. **(08 Marks)**

OR

4 a. Explain in brief : i) message switching ii) circuit switching. **(08 Marks)**

b. Explain electronic switching along with different facilities provided. **(08 Marks)**

Module-3

5 a. Derive the Erlang's lost call formula with iterative application of recurrence relation. **(09 Marks)**

b. A group of 20 trunks provides a grade of service of 0.01 when offered 12E of traffic. How much is the grade of service improved if 2 extra trunks are added to the group? How much does the grade of service deteriorates if one trunk is out of service? **(07 Marks)**

OR

6 a. Design a grading for connecting 20 trunks to switches having ten outlets. **(08 Marks)**

b. Derive the expression for minimum number of cross points in a three stage network with M incoming trunks and N outgoing trunks for (M > N) case. **(08 Marks)**

Module-4

7 a. Explain Time-Space-Time switch with suitable diagram. **(08 Marks)**

b. Explain synchronization and frame alignment of PCM signals in digital exchange. **(08 Marks)**

OR

8 a. Briefly explain basic software architecture of a DSS. **(08 Marks)**

b. With the help of features flow diagram, explain call forwarding feature. **(08 Marks)**

Module-5

9 a. Describe the various organizational interfaces of DSS central office. **(10 Marks)**

b. Briefly explain strategy for improving software quality with diagram. **(06 Marks)**

OR

10 a. Explain generic switch hardware architecture with neat diagram. **(08 Marks)**

b. Write short note on : i) Reliability analysis ii) Recovery strategy. **(08 Marks)**

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15EC663

Sixth Semester B.E. Degree Examination, June/July 2019
Digital System Design using Virology

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Define the terms setup time, hold time and clock to output time of a flip-flop and what are the constraints imposed by these parameter on the circuit operations. **(05 Marks)**

b. Develop veriology module for 7 segment decoder. Include an additional input 'blank' that overrides the BCD input and causes all segments not to be lit. **(06 Marks)**

c. Explain functional verification and formal verification for a verilog module **(05 Marks)**

OR

2 a. What are the effects of capacitive loading and propagation delay on signal transitions between logic levels? **(08 Marks)**

b. Develop verilog module for 4 : 1 MUX. **(04 Marks)**

c. Explain general view of digital system with data path control section. **(04 Marks)**

Module-2

3 a. Design a 64k ×8 bit composite memory using four 16k × 8 bit components and also explain how memory components with tristate data outputs simplify the construction of larger memories. **(08 Marks)**

b. Explain asynchronous static RAM with timing diagrams. **(08 Marks)**

OR

4 a. Write a note on multiport memories. **(08 Marks)**

b. Explain error detection and correction with one example. **(08 Marks)**

Module-3

5 a. Explain different types of PCB design. **(05 Marks)**

b. Explain implementation fabrics for digital system based on integrated circuit. **(07 Marks)**

c. What are EMI and cross talk? **(04 Marks)**

OR

6 a. Briefly explain programmable array logic. **(08 Marks)**

b. Explain signal integrity issue in PCB design and also explain measures to reduce these issues. **(08 Marks)**

Module-4

7 a. Explain the serial transmission of 64 bit data within clock domain with timing diagram. **(08 Marks)**

b. Explain the following serial interface standards for connecting I/O devices.
i) RS232 ii) Fire wire. **(08 Marks)**

OR

8 a. Explain any 4 analog sensors. **(08 Marks)**

b. Explain the concept of multiplexed buses **(08 Marks)**

Module-5

9 a. Explain logical partitioning and physical partitioning of a transport monitoring system. **(08 Marks)**

b. Explain fault model and fault simulation. **(08 Marks)**

OR

10 a. Explain 4 bit LFSR and CFSR for generating pseudorandom test vectors. **(08 Marks)**

b. Explain briefly area, power and timing optimization in digital circuits. **(08 Marks)**

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